

**EDP-CM-LPC1768 Command Module
User Manual**

Version 2.02

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1. Introduction

The RS-EDP platform is a system, has been designed to utilise many different manufacturers' microprocessors. To support NXP range or ARM/Cortex MCU's a single Command Module (CM) has been designed to accommodate four different device types. These are LPC2368 (ARM7), LPC1768 (Cortex M3), LPC1343 (Cortex M3) and LPC1113 (Cortex M0).

Each of the boards come with its own suite of software to fully exercise the RS-EDP Application Modules and the peripherals available on the MCU device.

In an RS-EDP system there is usually one Command Module (CM) and one or more Applications Modules (AM) plugged in to the Base Board (BB). These NXP modules have been designed as the Command Module for the system.

The 'Command Module' in a system dictates whether the whole system is a 3.3V one or a 5.0V one. All of these modules use a 3.3V microprocessor and consequently the I/O is mostly 3.3V also. To tell the rest of the system the Command Module is a 3.3V one not a 5.0V one, the Vcc_CM line on the base board is connected to 3.3V by the tracking on the Command Module board. This Vcc_CM is used as a reference by the other modules, such as the analogue module, to limit the output voltage to 3.3V. The command voltage line is also used by the #RESET circuit, as the voltage reference to pull up to after the reset line has been asserted low.

The RS-EDP-CM-NXP module maps the I/O of the MCU on the board to the backplane of the RS-EDP system. As there are quite a few dual function pins on the NXP processors and hence several link options have been made to accommodate the various options the user may wish to use. Extensive use of the I2C capability is used to communicate to the application modules in the system.

2. MCU Mapping

2.1 MCU Pin Allocation

The MCU pins have been connected to the backplane via the following configuration.

| LPC1768BDM100 | | Comment | RS-EDP-BASE BOARD - mapping |
|---------------|---------------------------------|------------------------------|-----------------------------|
| Pin | Name | | Name |
| 1 | TDO/SWO | JTAG interface on LPC module | |
| 2 | TDI | JTAG interface on LPC module | |
| 3 | TMS/SWDIO | JTAG interface on LPC module | |
| 4 | #TRST | JTAG interface on LPC module | |
| 5 | TCK/SWDCLK | JTAG interface on LPC module | |
| 6 | P0[26]/AD0[3]/AOUT/RXD3 | 3 link options | AN3 |
| | | 3 link options | AN11 |
| | | 3 link options | CPU_DAC00_GPIO17 |
| 7 | P0[25]/AD0[2]/I2SRX_SDA/TXD3 | 2 link options | AN2 |
| | | 2 link options | AN10 |
| 8 | P0[24]/AD0[1]/I2SRX_WS/CAP3[1] | 2 link options | AN1 |
| | | 2 link options | AN9 |
| 9 | P0[23]/AD0[0]/I2SRX_CLK/CAP3[0] | 2 link options | AN0 |
| | | 2 link options | AN8 |
| 10 | Vdda | 2 link options | AN_REF |
| | | 2 link options | Vcc_CM |
| 11 | Vssa | | VAGND |
| | | Jumper option to SGND | SGND |
| 12 | VREFP | 2 link options | AN_REF |

| | | | |
|----|-----------------------------------|----------------------------|---------------|
| | | 2 link options | Vcc_CM |
| 13 | NC | | 3.3V |
| 14 | #RSTOUT | | #RESOUT |
| 15 | VREFN | | VAGND |
| | | Jumper option to SGND | SGND |
| 16 | RTCX1 | 32KHz clock on LPC module | |
| 17 | #RESET | | #RESIN |
| 18 | STCX2 | 32KHz clock on LPC module | |
| 19 | VBAT | 2 link options | 3V BAT |
| | | 2 link options | 3.3V |
| 20 | P1[31]/SCK1/AD0[5] | 2 link options | AN5 |
| | | 2 link options | AN13 |
| 21 | P1[30]/Vbus/AD0[4] | 2 link options | AN4 |
| | | 2 link options | AN12 |
| 22 | XTAL1 | Xtal on module | |
| 23 | XTAL2 | Xtal on module | |
| 24 | P0[28]/SCL0/USB_SCL | | CNTRL_I2C_SCL |
| 25 | P0[27]/SDA0/USB_SDA | | CNTRL_I2C_SDA |
| | | | |
| 26 | P3[26]/STCLK/MAT0[1]/PWM1[3] | | EVG1_GPIO42 |
| | | | |
| 27 | P3[25]/MAT0[0]/PWM1[2] | 2 link options | EVG0_GPIO40 |
| | | 2 Link options - User LED1 | |
| 28 | Vdd(3V3) | | 3.3V |
| 29 | P0[29]/USB_D+ | | USB_DEV_D+ |
| 30 | P0[30]/USB_D- | | USB_DEV_D- |
| 31 | Vss | | SGND |
| 32 | P1[18]/USB_UP_LED/PWM1[1]/CAP1[0] | 3 link options | EVG5_GPIO50 |
| | | 3 link options | EVG8_GPIO56 |
| | | 3 link options | EVG0_GPIO40 |
| 33 | P1[19]/MCOA/USB_PPWR/CAP1[1] | 2 link options | MOTORP0H |
| | | 2 link options | EVG9_GPIO57 |
| 34 | P1[20]/MCFB0/PWM1[2]/SCK0 | 2 link options | MOTORH0_ENC0 |
| | | 2 link options | EVG10_GPIO58 |
| 35 | P1[21]/MCABORT/PWM1[3]/SSEL0 | 2 link options | EMG_TRAP |
| | | 2 link options | EVG11_GPIO59 |
| 36 | P1[22]/MCOB/USB_PWRD/MAT1[0] | 2 link options | MOTORP0L |
| | | 2 link options | EVG12_GPIO60 |
| 37 | P1[23]/MCFB1/PWM1[4]/MISO0 | 2 link options | MOTORH1_ENC1 |
| | | 2 link options | EVG13_GPIO61 |
| 38 | P1[24]/MCFB2/PWM1[5]/MOSI0 | 2 link options | MOTORH2_ENC2 |
| | | 2 link options | EVG14_GPIO62 |
| 39 | P1[25]/MC1A/MAT1[1] | 2 link options | MOTORP1H |
| | | 2 link options | EVG15_GPIO63 |
| 40 | P1[26]/MC1B/PWM1[6]/CAP0[0] | 2 link options | MOTORP1L |
| | | 2 link options | EVG16_GPIO64 |
| 41 | Vss | | SGND |
| 42 | Vdd(reg)(3V3) | | 3.3V |
| 43 | P1[27]/CLKOUT/USB_OVRRCR/CAP0[1] | | EVM5_GPIO47 |
| 44 | P1[28]/MC2A/PCAP1[0]/MAT0[0] | 2 link options | MOTORP2H |
| | | 2 link options | EVG17_GPIO65 |
| 45 | P1[29]/MC2B/PCAP1[1]/MAT0[1] | 2 link options | MOTORP2L |
| | | 2 link options | EVG18_GPIO66 |
| 46 | P0[0]/RD1/TXD3/SDA1 | 3 link options | CAN0_TX |
| | | 3 link options | CAN0_TX_LOCAL |
| | | 3 link options | I2C_GEN0_SDA |
| 47 | P0[1]/TD1/RXD3/SCL1 | 3 link options | CAN0_RX |
| | | 3 link options | CAN0_RX_LOCAL |
| | | 3 link options | I2C_GEN0_SCL |
| 48 | P0[10]/TXD2/SDA2/MAT3[0] | 2 link options | GPIO0 |
| | | 2 link options | EVG6_GPIO52 |

| | | | |
|----|---------------------------------|---------------------------|--------------------------|
| 49 | P0[11]/RXD2/SCL2/MAT3[1] | 2 link options | GPIO1 |
| | | 2 link options | EVG7_GPIO54 |
| 50 | P2[13]/#EINT3/I2STX_SDA | | GPIO8_MCI_DAT3 |
| 51 | P2[12]/#EINT2/I2STX_WS | | GPIO6_MCI_DAT2 |
| 52 | P2[11]/#EINT1/I2STX_CLK | | GPIO4_MCI_DAT1 |
| 53 | P2[10]/#EINT0/NMI | 2 link options | IRQ_GPIO16_CNTRL_I2C_INT |
| | | 2 link options | IRQ_GPIO18_I2C_GEN0_INT |
| 54 | Vdd(3V3) | | 3.3V |
| 55 | Vss | | SGND |
| 56 | P0[22]/RTS1/TD1 | 2 link options | GPIO2_MCI_DAT0 |
| | | 2 Link options | EVM6_GPIO49 |
| 57 | P0[21]/RI1/RD1 | 2 link options | GPIO14_MCI_PWR |
| | | 2 Link options | EVM4_GPIO45 |
| 58 | P0[20]/DTR1/SCL1 | 2 link options | GPIO12_MCI_CMD |
| | | 2 Link options | EVM3_GPIO43 |
| 59 | P0[19]/DSR1/SDA1 | 2 link options | GPIO10_MCI_CLK |
| | | 2 Link options | EVM2_GPIO41_CAPADC |
| 60 | P0[18]/DCD1/MOSI0/MOSI | | CNTRL_SPI_MTSR |
| 61 | P0[17]/CTS1/MISO0/MISO | | CNTRL_SPI_MRST |
| 62 | P0[15]/TXD1/SCK0/SCK | | CNTRL_SPI_CLK |
| 63 | P0[16]/RXD1/SSEL0/SSEL | | CNTRL_SPI_#CS_NSS |
| 64 | P2[9]/USB_CONNECT/RXD2 | 2 link options | ASC1_RX_TTL |
| | | 2 link options | EVM10_GPIO68_ASC0_CTS |
| 65 | P2[8]/TD2/TXD2 | 2 link options | ASC1_TX_TTL |
| | | 2 link options | CAN1_TX |
| 66 | P2[7]/RD2/RTS1 | 2 link options | ASC1_TX_TTL_ASC0_DTR |
| | | 2 link options | CAN1_RX |
| 67 | P2[6]/PCAP1[0]/RI1/TRACECLK | 2 link option | MOTOR_TCO_FB |
| | | 2 link options User LED0 | |
| 68 | P2[5]/PWM1[6]/DTR1/TRACEDATA[0] | 2 link option | EVG4_GPIO48 |
| | | 2 link option | EVG19_GPIO67 |
| 69 | P2[4]/PWM1[5]/DSR1/TRACEDATA[1] | 2 link option | CPU_DAC01_GPIO19 |
| | | 2 link option | EVG3_GPIO46 |
| 70 | P2[3]/PWM1[4]/DCD1/TRACEDATA[2] | 2 link option | CPU_DAC00_GPIO17 |
| | | 2 link option | EVG2_GPIO44 |
| 71 | Vdd(3V3) | | 3.3V |
| 72 | Vss | | SGND |
| 73 | P2[2]/PWM1[3]/CTS1/TRACEDATA[3] | | EVM9_GPIO55 |
| 74 | P2[1]/PWM1[2]/RXD1 | 2 link options | ASC1_RX_TTL |
| | | 2 Link options | EVM8_GPIO53 |
| 75 | P2[0]/PWM1[1]/TXD1 | 2 link options | ASC1_TX_TTL |
| | | 2 Link options | EVM7_GPIO51 |
| 76 | P0[9]/I2STX_SDA/MOSI1/MAT2[3] | Local_SD_SPI_MOSI | |
| 77 | P0[8]/I2STX_WS/MISO1/MAT2[2] | Local_SD_SPI_MISO | |
| 78 | P0[7]/I2STX_CLK/SCK1/MAT2[1] | Local_SD_SPICLK | |
| 79 | P0[6]/I2SRX_SDA/SSEL1/MAT2[0] | Local_SD_CS_SD | |
| 80 | P0[5]/I2SRX_WS/TD2/CAP2[1] | 3 link options | GPIO9_I2S_RX_WS |
| | | 3 link options | EVM1_GPIO23 |
| | | 3 link options | CPU_DAC00_GPIO17 |
| 81 | P0[4]/I2SRX_CLK/RD2/CAP2[0] | 2 link option | GPIO7_I2S_RX_CLK |
| | | 2 Link options | EVM0_GPIO21 |
| 82 | P4[28]/RX_MCLK/MAT2[0]/TXD3 | USB Debug ports FTDI chip | |
| 83 | Vss | | SGND |
| 84 | Vdd(reg)(3V3) | | 3.3V |
| 85 | P4[29]/TX_MCLK/MAT2[1]/RXD3 | USB Debug ports FTDI chip | |
| 86 | P1[17]/ENET_MDIO | Ethernet PHY chip | |
| 87 | P1[16]/ENET_MDC | Ethernet PHY chip | |
| 88 | P1[15]/ENET_REF_CLK | Ethernet PHY chip | |
| 89 | P1[14]/ENET_RX_ER | Ethernet PHY chip | |
| 90 | P1[10]/ENET_RXD1 | Ethernet PHY chip | |
| 91 | P1[9]/ENET_RXD0 | Ethernet PHY chip | |

| | | | |
|-----|-------------------|------------------------------|-------------|
| 92 | P1[8]/ENET_CRS | Ethernet PHY chip | |
| 93 | P1[4]/ENET_TX_EN | Ethernet PHY chip | |
| 94 | P1[1]/ENET_TXD1 | Ethernet PHY chip | |
| 95 | P1[0]/ENET_TXD0 | Ethernet PHY chip | |
| 96 | Vdd(3V3) | | 3.3V |
| 97 | Vss | | SGND |
| 98 | P0[2]/TXD0/AD0[7] | 3 Link options | ASC0_TX_TTL |
| | | 3 link options | AN7 |
| | | 3 link options | AN15 |
| 99 | P0[3]/RXD0/AD0[6] | 3 Link options | ASC0_RX_TTL |
| | | 3 link options | AN6 |
| | | 3 link options | AN14 |
| 100 | RTCK | JTAG interface on LPC module | |

2.2 Resources Used/Available by the LPC1768

The following resources are available to be used by the MCU

| Resources Used/Available |
|--------------------------|
| 3.3V |
| 3V BAT |
| Vcc_CM |
| AN_REF |
| VAGND |
| #RESIN |
| #RESOUT |
| SGND |
| VAGND |
| AN0 |
| AN1 |
| AN2 |
| AN3 |
| AN4 |
| AN5 |
| AN6 |
| AN7 |
| AN8 |
| AN9 |
| AN10 |
| AN11 |
| AN12 |
| AN13 |
| AN14 |
| AN15 |
| ASC0_RX_TTL |
| ASC0_TX_TTL |
| ASC1_RX_TTL |
| ASC1_TX_TTL |
| ASC1_TX_TTL_ASC0_DTR |
| CAN0_RX |
| CAN0_TX |
| CAN1_RX |
| CAN1_TX |
| CAN0H |
| CAN0L |
| CNTRL_I2C_SCL |
| CNTRL_I2C_SDA |
| CNTRL_SPI_#CS_NSS |

| |
|--------------------------|
| CNTRL_SPI_CLK |
| CNTRL_SPI_MRST |
| CNTRL_SPI_MTSR |
| CPU_DAC00_GPIO17 |
| CPU_DAC00_GPIO17 |
| CPU_DAC01_GPIO19 |
| EVG0_GPIO40 |
| EVG1_GPIO42 |
| EVG2_GPIO44 |
| EVG3_GPIO46 |
| EVG4_GPIO48 |
| EVG5_GPIO50 |
| EVG6_GPIO52 |
| EVG7_GPIO54 |
| EVG8_GPIO56 |
| EVG9_GPIO57 |
| EVG10_GPIO58 |
| EVG11_GPIO59 |
| EVG12_GPIO60 |
| EVG13_GPIO61 |
| EVG14_GPIO62 |
| EVG15_GPIO63 |
| EVG16_GPIO64 |
| EVG17_GPIO65 |
| EVG18_GPIO66 |
| EVG19_GPIO67 |
| EVM0_GPIO21 |
| EVM1_GPIO23 |
| EVM2_GPIO41_CAPADC |
| EVM3_GPIO43 |
| EVM4_GPIO45 |
| EVM5_GPIO47 |
| EVM6_GPIO49 |
| EVM7_GPIO51 |
| EVM8_GPIO53 |
| EVM9_GPIO55 |
| EVM10_GPIO68_ASC0_CTS |
| GPIO0 |
| GPIO1 |
| GPIO7_I2S_RX_CLK |
| GPIO9_I2S_RX_WS |
| GPIO10_MCI_CLK |
| GPIO12_MCI_CMD |
| GPIO14_MCI_PWR |
| GPIO2_MCI_DAT0 |
| GPIO4_MCI_DAT1 |
| GPIO6_MCI_DAT2 |
| GPIO8_MCI_DAT3 |
| I2C_GEN0_SCL |
| I2C_GEN0_SDA |
| IRQ_GPIO16_CNTRL_I2C_INT |
| IRQ_GPIO18_I2C_GEN0_INT |
| MOTORP0H |
| MOTORP0L |
| MOTORP1H |
| MOTORP1L |
| MOTORP2H |
| MOTORP2L |
| MOTORH0_ENC0 |
| MOTORH1_ENC1 |
| MOTORH2_ENC2 |

| |
|--------------|
| EMG_TRAP |
| MOTOR_TCO_FB |
| USB_DEV_D- |
| USB_DEV_D+ |

2.3 Alphabetical Listing of MCU pins

| Pin | Alphabetic Listing of Available I/O |
|-----|-------------------------------------|
| 17 | #RESET |
| 14 | #RSTOUT |
| 4 | #TRST |
| 13 | NC |
| 46 | P0[0]/RD1/TXD3/SDA1 |
| 47 | P0[1]/TD1/RXD3/SCL1 |
| 98 | P0[2]/TXD0/AD0[7] |
| 99 | P0[3]/RXD0/AD0[6] |
| 81 | P0[4]/I2SRX_CLK/RD2/CAP2[0] |
| 80 | P0[5]/I2SRX_WS/TD2/CAP2[1] |
| 79 | P0[6]/I2SRX_SDA/SSEL1/MAT2[0] |
| 78 | P0[7]/I2STX_CLK/SCK1/MAT2[1] |
| 77 | P0[8]/I2STX_WS/MISO1/MAT2[2] |
| 76 | P0[9]/I2STX_SDA/MOSI1/MAT2[3] |
| 48 | P0[10]/TXD2/SDA2/MAT3[0] |
| 49 | P0[11]/RXD2/SCL2/MAT3[1] |
| 62 | P0[15]/TXD1/SCK0/SCK |
| 63 | P0[16]/RXD1/SSELO/SSEL |
| 61 | P0[17]/CTS1/MISO0/MISO |
| 60 | P0[18]/DCD1/MOSI0/MOSI |
| 59 | P0[19]/DSR1/SDA1 |
| 58 | P0[20]/DTR1/SCL1 |
| 57 | P0[21]/R1/RD1 |
| 56 | P0[22]/RTS1/TD1 |
| 9 | P0[23]/AD0[0]/I2SRX_CLK/CAP3[0] |
| 8 | P0[24]/AD0[1]/I2SRX_WS/CAP3[1] |
| 7 | P0[25]/AD0[2]/I2SRX_SDA/TXD3 |
| 6 | P0[26]/AD0[3]/AOUT/RXD3 |
| 25 | P0[27]/SDA0/USB_SDA |
| 24 | P0[28]/SCL0/USB_SCL |
| 29 | P0[29]/USB_D+ |
| 30 | P0[30]/USB_D- |
| 95 | P1[0]/ENET_TXD0 |
| 94 | P1[1]/ENET_TXD1 |
| 93 | P1[4]/ENET_TX_EN |
| 92 | P1[8]/ENET_CRS |
| 91 | P1[9]/ENET_RXD0 |
| 90 | P1[10]/ENET_RXD1 |
| 89 | P1[14]/ENET_RX_ER |
| 88 | P1[15]/ENET_REF_CLK |
| 87 | P1[16]/ENET_MDC |
| 86 | P1[17]/ENET_MDIO |
| 32 | P1[18]/USB_UP_LED/PWM1[1]/CAP1[0] |
| 33 | P1[19]/MCOA/USB_PPWR/CAP1[1] |
| 34 | P1[20]/MCFB0/PWM1[2]/SCK0 |
| 35 | P1[21]/MCABORT/PWM1[3]/SSELO |
| 36 | P1[22]/MCOB/USB_PWRD/MAT1[0] |
| 37 | P1[23]/MCFB1/PWM1[4]/MISO0 |
| 38 | P1[24]/MCFB2/PWM1[5]/MOSI0 |
| 39 | P1[25]/MC1A/MAT1[1] |
| 40 | P1[26]/MC1B/PWM1[6]/CAP0[0] |

| | |
|-----|---------------------------------|
| 43 | P1[27]/CLKOUT/USB_OVRCR/CAPO[1] |
| 44 | P1[28]/MC2A/PCAP1[0]/MATO[0] |
| 45 | P1[29]/MC2B/PCAP1[1]/MATO[1] |
| 21 | P1[30]/Vbus/AD0[4] |
| 20 | P1[31]/SCK1/AD0[5] |
| 75 | P2[0]/PWM1[1]/TXD1 |
| 74 | P2[1]/PWM1[2]/RXD1 |
| 73 | P2[2]/PWM1[3]/CTS1/TRACEDATA[3] |
| 70 | P2[3]/PWM1[4]/DCD1/TRACEDATA[2] |
| 69 | P2[4]/PWM1[5]/DSR1/TRACEDATA[1] |
| 68 | P2[5]/PWM1[6]/DTR1/TRACEDATA[0] |
| 67 | P2[6]/PCAP1[0]/RI1/TRACECLK |
| 66 | P2[7]/RD2/RTS1 |
| 65 | P2[8]/TD2/TXD2 |
| 64 | P2[9]/USB_CONNECT/RXD2 |
| 53 | P2[10]/#EINT0/NMI |
| 52 | P2[11]/#EINT1/I2STX_CLK |
| 51 | P2[12]/#EINT2/I2STX_WS |
| 50 | P2[13]/#EINT3/I2STX_SDA |
| 27 | P3[25]/MATO[0]/PWM1[2] |
| 26 | P3[26]/STCLK/MATO[1]/PWM1[3] |
| 82 | P4[28]/RX_MCLK/MAT2[0]/TXD3 |
| 85 | P4[29]/TX_MCLK/MAT2[1]/RXD3 |
| 100 | RTCK |
| 16 | RTCX1 |
| 18 | STCX2 |
| 5 | TCK/SWDCLK |
| 2 | TDI |
| 1 | TDO/SWO |
| 3 | TMS/SWDIO |
| 19 | VBAT |
| 28 | Vdd(3V3) |
| 54 | Vdd(3V3) |
| 71 | Vdd(3V3) |
| 96 | Vdd(3V3) |
| 42 | Vdd(reg)(3V3) |
| 84 | Vdd(reg)(3V3) |
| 10 | Vdda |
| 15 | VREFN |
| 12 | VREFP |
| 31 | Vss |
| 41 | Vss |
| 55 | Vss |
| 72 | Vss |
| 83 | Vss |
| 97 | Vss |
| 11 | Vssa |
| 22 | XTAL1 |
| 23 | XTAL2 |

2.4 Backplane Signal Names and Connections

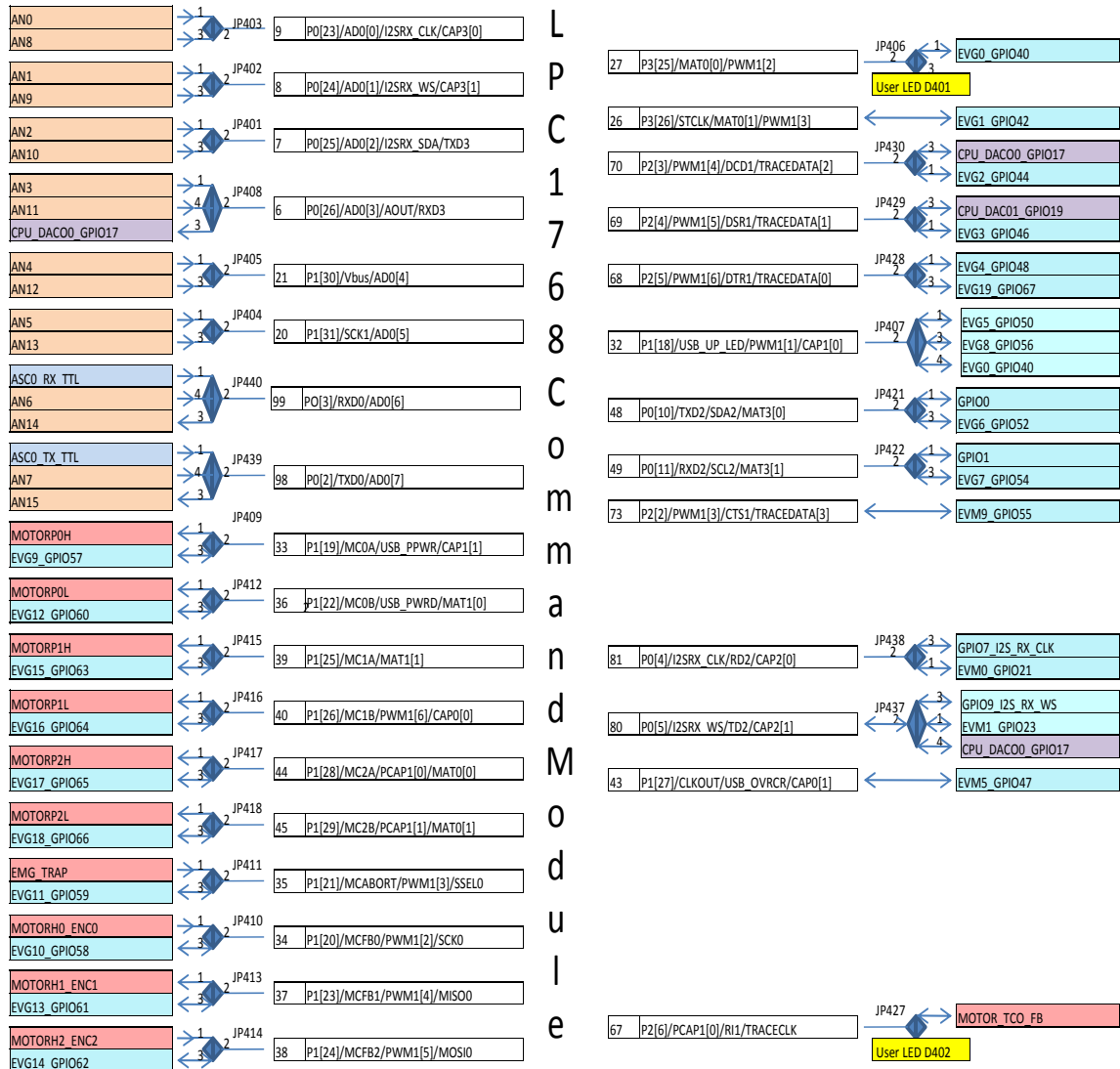
| Base Board Signal Name | EDPCON1 | EDPCON2 | Break Out Connector | |
|------------------------|---------|---------|---------------------|--|
| #CS0 | | 53 & 54 | | |
| #CS1 | | 55 & 56 | | |
| #CS2 | | 57 & 58 | | |
| #CS3 | | 59 & 60 | | |
| #PSEN | | 51 & 52 | | |
| #RD | | 45 & 46 | | |

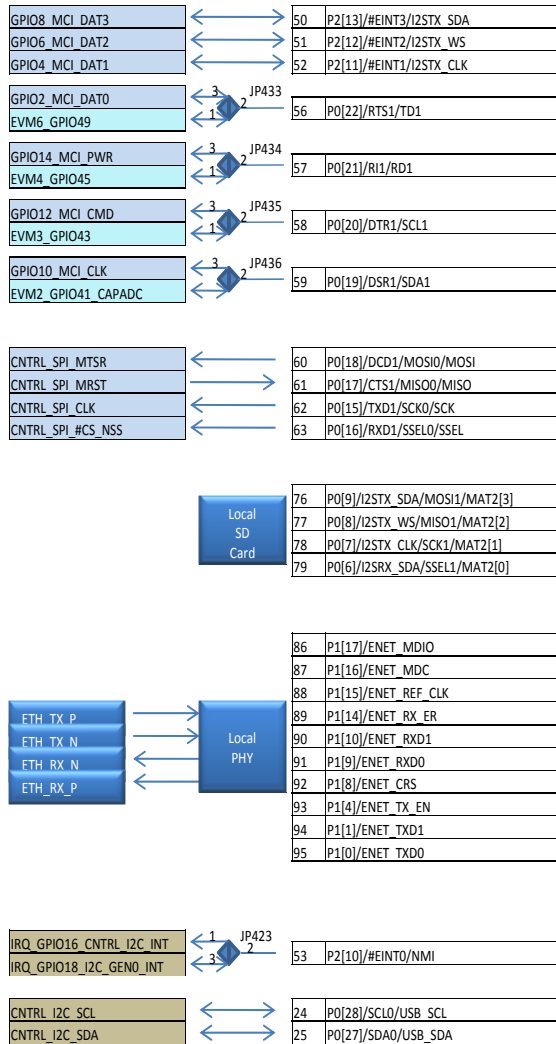
| | | | | |
|----------------------|-----|---------|------|----|
| #RESIN | | 1 & 2 | P603 | 26 |
| #RESQUT | | 3 & 4 | P603 | 27 |
| #WR | | 47 & 48 | | |
| #WRH | | 49 & 50 | | |
| 12V | 133 | | P603 | 47 |
| 12V | 134 | | P603 | 47 |
| 12V | 135 | | P603 | 47 |
| 12V | 136 | | P603 | 47 |
| 12V GND | 137 | | P603 | 48 |
| 12V GND | 138 | | P603 | 48 |
| 12V GND | 139 | | P603 | 48 |
| 12V GND | 140 | | P603 | 48 |
| 3.3V | 127 | | P603 | 44 |
| 3.3V | 128 | | P603 | 44 |
| 3.3V | | 95 & 96 | P603 | 44 |
| 3V BAT | 124 | | P603 | 42 |
| 5.0V | 129 | | P603 | 45 |
| 5.0V | 130 | | P603 | 45 |
| 5.0V | | 97 & 98 | P603 | 45 |
| A0_AD0 | | 41 & 42 | | |
| A1_AD1 | | 39 & 40 | | |
| A2_AD2 | | 37 & 38 | | |
| A3_AD3 | | 35 & 36 | | |
| A4_AD4 | | 33 & 34 | | |
| A5_AD5 | | 31 & 32 | | |
| A6_AD6 | | 29 & 30 | | |
| A7_AD7 | | 27 & 28 | | |
| A8_AD8 | | 25 & 26 | | |
| A9_AD9 | | 23 & 24 | | |
| A10_AD10 | | 21 & 22 | | |
| A11_AD11 | | 19 & 20 | | |
| A12_AD12 | | 17 & 18 | | |
| A13_AD13 | | 15 & 16 | | |
| A14_AD14 | | 13 & 14 | | |
| A15_AD15 | | 11 & 12 | | |
| ALE | | 43 & 44 | | |
| AN_REF | 1 | | P601 | 6 |
| AN0 | 3 | | P603 | 2 |
| AN1 | 4 | | P603 | 6 |
| AN2 | 5 | | P603 | 1 |
| AN3 | 6 | | P603 | 5 |
| AN4 | 7 | | P602 | 2 |
| AN5 | 8 | | P602 | 4 |
| AN6 | 9 | | P602 | 1 |
| AN7 | 10 | | P602 | 3 |
| AN8 | 11 | | P601 | 2 |
| AN9 | 12 | | P601 | 4 |
| AN10 | 13 | | P601 | 1 |
| AN11 | 14 | | P601 | 3 |
| AN12 | 15 | | P603 | 4 |
| AN13 | 16 | | P602 | 6 |
| AN14 | 17 | | P603 | 3 |
| AN15 | 18 | | P602 | 5 |
| ASC0_RX_TTL | 89 | | P602 | 30 |
| ASC0_TX_TTL | 91 | | P602 | 31 |
| ASC1_RX_TTL | 93 | | P602 | 32 |
| ASC1_RX_TTL_ASC0_DSR | 99 | | P602 | 35 |
| ASC1_TX_TTL | 95 | | P602 | 33 |
| ASC1_TX_TTL_ASC0_DTR | 97 | | P602 | 34 |
| CAN0_RX | | 61 & 62 | | |
| CAN0_TX | | 63 & 64 | | |

| | | | | |
|-----------------------|-----|---------|------|----|
| CAN1_RX | 121 | | P602 | 46 |
| CAN1_TX | 123 | | P602 | 47 |
| CANH0 | | 89 & 90 | P603 | 40 |
| CANL0 | | 91 & 92 | P603 | 41 |
| CNTRL_I2C_SCL | | 79 & 80 | P603 | 35 |
| CNTRL_I2C_SDA | | 77 & 78 | P603 | 34 |
| CNTRL_SPI_#CS_NSS | | 75 & 76 | P603 | 33 |
| CNTRL_SPI_CLK | | 69 & 70 | P603 | 30 |
| CNTRL_SPI_MRST | | 71 & 72 | P603 | 31 |
| CNTRL_SPI_MTSR | | 73 & 74 | P603 | 32 |
| CPU_DAC01_GPIO19 | 40 | | P601 | 7 |
| CPU_DAC00_GPIO17 | 38 | | P603 | 7 |
| EMG_TRAP | 114 | | P601 | 44 |
| ETH_LNK_LED | 111 | | P602 | 41 |
| ETH_RX- | 109 | | P602 | 40 |
| ETH_RX_LED | 113 | | P602 | 42 |
| ETH_RX+ | 107 | | P602 | 39 |
| ETH_SPD_LED | 115 | | P602 | 43 |
| ETH_TX- | 105 | | P602 | 38 |
| ETH_TX+ | 103 | | P602 | 37 |
| EVG0_GPIO40 | 61 | | P602 | 16 |
| EVG1_GPIO42 | 63 | | P602 | 17 |
| EVG2_GPIO44 | 65 | | P602 | 18 |
| EVG3_GPIO46 | 67 | | P602 | 19 |
| EVG4_GPIO48 | 69 | | P602 | 20 |
| EVG5_GPIO50 | 71 | | P602 | 21 |
| EVG6_GPIO52 | 73 | | P602 | 22 |
| EVG7_GPIO54 | 75 | | P602 | 23 |
| EVG8_GPIO56 | 77 | | P602 | 24 |
| EVG9_GPIO57 | 78 | | P601 | 26 |
| EVG10_GPIO58 | 79 | | P602 | 25 |
| EVG11_GPIO59 | 80 | | P601 | 27 |
| EVG12_GPIO60 | 81 | | P602 | 26 |
| EVG13_GPIO61 | 82 | | P601 | 28 |
| EVG14_GPIO62 | 83 | | P602 | 27 |
| EVG15_GPIO63 | 84 | | P601 | 29 |
| EVG16_GPIO64 | 85 | | P602 | 28 |
| EVG17_GPIO65 | 86 | | P601 | 30 |
| EVG18_GPIO66 | 87 | | P602 | 29 |
| EVG19_GPIO67 | 88 | | P601 | 31 |
| EVG20_GPIO69_ASCO_RTS | 92 | | P601 | 33 |
| EVM0_GPIO21 | 42 | | P601 | 8 |
| EVM1_GPIO23 | 44 | | P601 | 9 |
| EVM2_GPIO41_CAPADC | 62 | | P601 | 18 |
| EVM3_GPIO43 | 64 | | P601 | 19 |
| EVM4_GPIO45 | 66 | | P601 | 20 |
| EVM5_GPIO47 | 68 | | P601 | 21 |
| EVM6_GPIO49 | 70 | | P601 | 22 |
| EVM7_GPIO51 | 72 | | P601 | 23 |
| EVM8_GPIO53 | 74 | | P601 | 24 |
| EVM9_GPIO55 | 76 | | P601 | 25 |
| EVM10_GPIO68_ASCO_CTS | 90 | | P601 | 32 |
| GPIO0 | 21 | | P603 | 13 |
| GPIO1 | 22 | | P603 | 15 |
| GPIO2_MCI_DAT0 | 23 | | P603 | 14 |
| GPIO3 | 24 | | P603 | 16 |
| GPIO4_MCI_DAT1 | 25 | | P603 | 17 |
| GPIO5_I2S_TX_WS | 26 | | P603 | 19 |
| GPIO6_MCI_DAT2 | 27 | | P603 | 18 |
| GPIO7_I2S_RX_CLK | 28 | | P603 | 20 |
| GPIO8_MCI_DAT3 | 29 | | P603 | 22 |

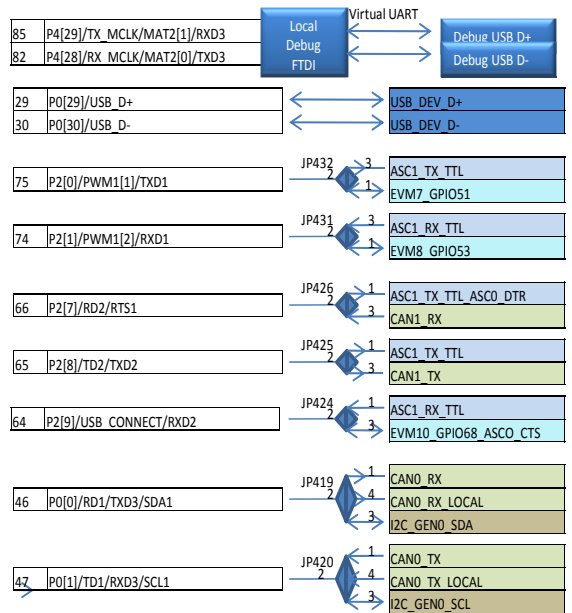
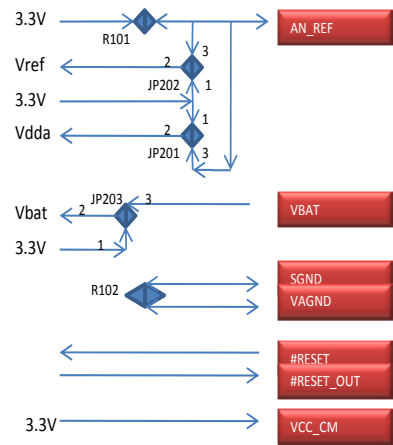
| | | | | |
|--------------------------|-----|----------|------|----|
| GPIO9_I2S_RX_WS | 30 | | P603 | 21 |
| GPIO10_MCI_CLK | 31 | | P603 | 23 |
| GPIO11_I2S_RX_SDA | 32 | | P603 | 24 |
| GPIO12_MCI_CMD | 33 | | | |
| GPIO13_I2S_TX_CLK | 34 | | P603 | 25 |
| GPIO14_MCI_PWR | 35 | | P603 | 12 |
| GPIO15_I2S_TX_SDA | 36 | | P603 | 8 |
| GPIO24_AD7 | 45 | | P602 | 8 |
| GPIO25_AD15 | 46 | | P601 | 10 |
| GPIO26_AD6 | 47 | | P602 | 9 |
| GPIO27_AD14 | 48 | | P601 | 11 |
| GPIO28_AD5 | 49 | | P602 | 10 |
| GPIO29_AD13 | 50 | | P601 | 12 |
| GPIO30_AD4 | 51 | | P602 | 11 |
| GPIO31_AD12 | 52 | | P601 | 13 |
| GPIO32_AD3 | 53 | | P602 | 12 |
| GPIO33_AD11 | 54 | | P601 | 14 |
| GPIO34_AD2 | 55 | | P602 | 13 |
| GPIO35_AD10 | 56 | | P601 | 15 |
| GPIO36_AD1 | 57 | | P602 | 14 |
| GPIO37_AD9 | 58 | | P601 | 16 |
| GPIO38_AD0 | 59 | | P602 | 15 |
| GPIO39_AD8 | 60 | | P601 | 17 |
| I2C_GEN0_SCL | | 7 & 8 | P603 | 29 |
| I2C_GEN0_SDA | | 5 & 6 | P603 | 28 |
| I2C_GEN1_SCL | 119 | | P602 | 45 |
| I2C_GEN1_SDA | 117 | | P602 | 44 |
| IRQ_GPIO16_CNTRL_I2C_INT | 37 | | P603 | 11 |
| IRQ_GPIO18_I2C_GEN0_INT | 39 | | P603 | 10 |
| IRQ_GPIO20_I2C_GEN1_INT | 41 | | P603 | 9 |
| IRQ_GPIO22_I2C_INT | 43 | | P602 | 7 |
| MOTOR_TCO_FB | 122 | | P601 | 48 |
| MOTORH0_ENC0 | 116 | | P601 | 45 |
| MOTORH1_ENC1 | 118 | | P601 | 46 |
| MOTORH2_ENC2 | 120 | | P601 | 47 |
| MOTORP0H | 102 | | P601 | 38 |
| MOTORP0L | 100 | | P601 | 37 |
| MOTORP1H | 106 | | P601 | 40 |
| MOTORP1L | 104 | | P601 | 39 |
| MOTORP2H | 110 | | P601 | 42 |
| MOTORP2L | 108 | | P601 | 41 |
| MOTORPWM | 112 | | P601 | 43 |
| SGND | 131 | | P603 | 46 |
| SGND | 132 | | P603 | 46 |
| SGND | | 9 & 10 | P603 | 46 |
| SGND | | 99 & 100 | P603 | 46 |
| SPI_SSC_CS_NSS | 101 | | P602 | 36 |
| SPI_SSC_CLK | 98 | | P601 | 36 |
| SPI_SSC_MRST_MISO | 94 | | P601 | 34 |
| SPI_SSC_MTSR_MOSI | 96 | | P601 | 35 |
| USB_DEBUG_D- | | 67 & 68 | | |
| USB_DEBUG_D+ | | 65 & 66 | | |
| USB_DEV_D- | | 87 & 88 | P603 | 39 |
| USB_DEV_D+ | | 85 & 86 | P603 | 38 |
| USB_HOST_D- | | 83 & 84 | P603 | 37 |
| USB_HOST_D+ | | 81 & 82 | P603 | 36 |
| VAGND | 19 | | P601 | 5 |
| VAGND | 20 | | P601 | 5 |
| Vcc_CM | 125 | | P603 | 43 |
| Vcc_CM | 126 | | P603 | 43 |
| Vcc_CM | | 93 & 94 | P603 | 43 |

2.5 Mapping Aids





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3. Solder Link Options

Many of the options for the Command Module board require a solder bridge to be made or a track to be cut. The CM board has been designed to be configured in the most popular setting by using a small track between the options, which will require cutting with a sharp knife before making the alternate connection options.

The options we have are as follows:

VDDA

| | |
|-------------|---|
| JP201 (1-2) | VDDA on the MCU is connected to 3.3V |
| JP201 (2-3) | VDDA on the MCU is connected to AN_REF on the backplane |

Vref

| | |
|-------------|--------------------------------------|
| JP202 (1-2) | VREF on the MCU is connected to 3.3V |
|-------------|--------------------------------------|

| | |
|-------------|---|
| JP202 (2-3) | VREF on the MCU is connected to AN_REF on the backplane |
|-------------|---|

VBAT

| | |
|-------------|---|
| JP203 (1-2) | VBAT on the MCU is connected to 3.3V |
| JP203 (2-3) | VREF on the MCU is connected to 3V3_BATT on the backplane |

Port P0 Options

P0[0]/RD1/TXD3/SDA1

| | |
|-----------------------|---------------|
| JP419 (2-1) | CAN0_TX |
| JP419 (2-4) (Default) | CAN0_TX_LOCAL |
| JP419 (2-3) | I2C_GEN0_SDA |

Position 2-1 puts the CAN logic level transmit traffic on the backplane. A physical layer CAN transceiver on the Communications Module can translate this in to the CANH and CANL physical layer for networking. It is possible on the Communications Module to make this CAN isolated.

Position 2-4 routes the CAN logic level transmit traffic to a local physical layer CAN transceiver on the NXP Command Module. The output of the CAN transceiver (CANH and CANL) is routed down the back plane to the Comms Module and output on a standard 9 way D connector.

Position 2-3 allows this pin to be used as a second I2C channel, I2C_GEN0.

P0[1]/TD1/RXD3/SCL1

| | |
|-----------------------|---------------|
| JP420 (2-1) | CAN0_RX |
| JP420 (2-4) (Default) | CAN0_RX_LOCAL |
| JP420 (2-3) | I2C_GEN0_SCL |

Position 2-1 routes the CAN logic level receive traffic from the backplane to the I/O pin. The traffic usually comes from the physical layer CAN transceiver present on the Communications Module. It is possible on the Comms Module to have an isolated CAN stream.

Position 2-4 routes the CAN logic level receive traffic from the local physical layer CAN transceiver on the NXP Command Module.

Position 2-3 allows this pin to be used as a second I2C channel, I2C_GEN0.

P0[2]/TXD0/AD0[7]

| | |
|-----------------------|-------------|
| JP439 (2-1) (Default) | ASC0_TX_TTL |
| JP439 (2-4) | AN7 |
| JP439 (2-3) | AN15 |

Position 2-1 is the main RS232/UART channel. Outgoing logic level transmit traffic is routed to the Communication Module where it is translated into RS232/RS485 logic levels.

P0[3]/RXD0/AD0[6]

| | |
|-----------------------|-------------|
| JP440 (2-1) (Default) | ASC0_RX_TTL |
| JP440 (2-4) | AN6 |
| JP440 (2-3) | AN14 |

Position 2-1 is the main RS232/UART channel. Incoming logic level receive traffic is routed from the Communication Module.

P0[4]/I2SRX_CLK/RD2/CAP2[0]

| | |
|-----------------------|------------------|
| JP438 (2-3) | GPIO7_I2S_RX_CLK |
| JP438 (2-1) (Default) | EVM0_GPIO21 |

P0[5]/I2SRX_WS/TD2/CAP2[1]

| | |
|-----------------------|------------------|
| JP437 (2-3) | GPIO9_I2S_RX_WS |
| JP437 (2-1) (Default) | EVM1_GPIO23 |
| JP437 (2-4) | CPU_DAC00_GPIO17 |

P0[10]/TXD2/SDA2/MAT3[0]

| | |
|-----------------------|-------------|
| JP421 (2-1) (Default) | GPIO0 |
| JP421 (2-3) | EVG6_GPIO52 |

P0[11]/RXD2/SCL2/MAT3[1]

| | |
|-----------------------|-------------|
| JP422 (2-1) (Default) | GPIO1 |
| JP422 (2-3) | EVG7_GPIO54 |

P0[19]/DSR1/SDA1

| | |
|-----------------------|--------------------|
| JP436 (2-3) | GPIO10_MCI_CLK |
| JP436 (2-1) (Default) | EVM2_GPIO41_CAPADC |

P0[20]/DTR1/SCL1

| | |
|-----------------------|----------------|
| JP435 (2-3) | GPIO12_MCI_CMD |
| JP435 (2-1) (Default) | EVM3_GPIO43 |

P0[21]/RI1/RD1

| | |
|-----------------------|----------------|
| JP434 (2-3) | GPIO14_MCI_PWR |
| JP434 (2-1) (Default) | EVM4_GPIO45 |

P0[22]/RTS1/TD1

| | |
|-----------------------|----------------|
| JP433 (2-3) | GPIO2_MCI_DAT0 |
| JP433 (2-1) (Default) | EVM6_GPIO49 |

P0[23]/AD0[0]/I2SRX_CLK/CAP3[0]

| | |
|-----------------------|-----|
| JP403 (2-1) (Default) | AN0 |
| JP403 (2-3) | AN8 |

P0[24]/AD0[1]/I2SRX_WS/CAP3[1]

| | |
|-----------------------|-----|
| JP402 (2-1) (Default) | AN1 |
| JP402 (2-3) | AN9 |

P0[25]/AD0[2]/I2SRX_SDA/TXD3

| | |
|-----------------------|------|
| JP401 (2-1) (Default) | AN2 |
| JP401 (2-3) | AN10 |

P0[26]/AD0[3]/AOUT/RXD3

| | |
|-----------------------|------------------|
| JP408 (2-1) (Default) | AN3 |
| JP408 (2-4) | AN11 |
| JP408 (2-3) | CPU_DAC00_GPIO17 |

Port P1 Options

P1[18]/USB_UP_LED/PWM1[1]/CAP1[0]

| | |
|-----------------------|-------------|
| JP407 (2-1) (Default) | EVG5_GPIO50 |
| JP407 (2-3) | EVG8_GPIO56 |
| JP407 (2-4) | EVG0_GPIO40 |

P1[19]/MC0A/USB_PPWR/CAP1[1]

| | |
|-----------------------|-------------|
| JP409 (2-1) | MOTORP0H |
| JP409 (2-3) (Default) | EVG9_GPIO57 |

P1[20]/MCFB0/PWM1[2]/SCK0

| | |
|-----------------------|--------------|
| JP410 (2-1) | MOTORH0_ENC0 |
| JP410 (2-3) (Default) | EVG10_GPIO58 |

P1[21]/MCABORT/PWM1[3]/SSELO

| | |
|-----------------------|--------------|
| JP411 (2-1) | EMG_TRAP |
| JP411 (2-3) (Default) | EVG11_GPIO59 |

P1[22]/MCOB/USB_PWRD/MAT1[0]

| | |
|-----------------------|--------------|
| JP412 (2-1) | MOTORP0L |
| JP412 (2-3) (Default) | EVG12_GPIO60 |

P1[23]/MCFB1/PWM1[4]/MISO0

| | |
|-----------------------|--------------|
| JP413 (2-1) | MOTORH1_ENC1 |
| JP413 (2-3) (Default) | EVG13_GPIO61 |

P1[24]/MCFB2/PWM1[5]/MOSI0

| | |
|-----------------------|--------------|
| JP414 (2-1) | MOTORH2_ENC2 |
| JP414 (2-3) (Default) | EVG14_GPIO62 |

P1[25]/MC1A/MAT1[1]

| | |
|-----------------------|--------------|
| JP415 (2-1) | MOTORP1H |
| JP415 (2-3) (Default) | EVG15_GPIO63 |

P1[26]/MC1B/PWM1[6]/CAPO[0]

| | |
|-----------------------|--------------|
| JP416 (2-1) | MOTORP1L |
| JP416 (2-3) (Default) | EVG16_GPIO64 |

P1[28]/MC2A/PCAP1[0]/MAT0[0]

| | |
|-----------------------|--------------|
| JP417 (2-1) | MOTORP2H |
| JP417 (2-3) (Default) | EVG17_GPIO65 |

P1[29]/MC2B/PCAP1[1]/MAT0[1]

| | |
|-----------------------|--------------|
| JP418 (2-1) | MOTORP2L |
| JP418 (2-3) (Default) | EVG18_GPIO66 |

P1[30]/Vbus/AD0[4]

| | |
|-----------------------|------|
| JP405 (2-1) (Default) | AN4 |
| JP405 (2-3) | AN12 |

P1[31]/SCK1/AD0[5]

| | |
|-----------------------|------|
| JP404 (2-1) (Default) | AN5 |
| JP404 (2-3) | AN13 |

Port P2 Options**P2[0]/PWM1[1]/TXD1**

| | |
|-----------------------|-------------|
| JP432 (2-3) | ASC1_TX_TTL |
| JP432 (2-1) (Default) | EVM7_GPIO51 |

P2[1]/PWM1[2]/RXD1

| | |
|-----------------------|-------------|
| JP431 (2-3) | ASC1_RX_TTL |
| JP431 (2-1) (Default) | EVM8_GPIO53 |

P2[3]/PWM1[4]/DCD1/TRACEDATA[2]

| | |
|-----------------------|------------------|
| JP430 (2-3) | CPU_DAC00_GPIO17 |
| JP430 (2-1) (Default) | EVG2_GPIO44 |

P2[4]/PWM1[5]/DSR1/TRACEDATA[1]

| | |
|-----------------------|------------------|
| JP429 (2-3) | CPU_DAC01_GPIO19 |
| JP429 (2-1) (Default) | EVG3_GPIO46 |

P2[5]/PWM1[6]/DTR1/TRACEDATA[0]

| | |
|-----------------------|--------------|
| JP428 (2-1) (Default) | EVG4_GPIO48 |
| JP428 (2-3) | EVG19_GPIO67 |

P2[6]/PCAP1[0]/RI1/TRACECLK

| | |
|-----------------------|--------------|
| JP427 (2-1) | MOTOR_TCO_FB |
| JP427 (2-3) (Default) | User LED0 |

P2[7]/RD2/RTS1

| | |
|-----------------------|----------------------|
| JP426 (2-1) (Default) | ASC1_TX_TTL_ASC0_DTR |
| JP426 (2-3) | CAN1_RX |

P2[8]/TD2/TXD2

| | |
|-----------------------|-------------|
| JP425 (2-1) (Default) | ASC1_TX_TTL |
| JP425 (2-3) | CAN1_TX |

P2[9]/USB_CONNECT/RXD2

| | |
|-----------------------|-----------------------|
| JP424 (2-1) (Default) | ASC1_RX_TTL |
| JP424 (2-3) | EVM10_GPIO68_ASC0_CTS |

P2[10]/#EINT0/NMI

| | |
|-----------------------|--------------------------|
| JP423 (2-1) (Default) | IRQ_GPIO16_CNTRL_I2C_INT |
| JP423 (2-3) | IRQ_GPIO18_I2C_GEN0_INT |

Port P3 Options**P3[25]/MAT0[0]/PWM1[2]**

| | |
|-------------|-------------|
| JP406 (2-1) | EVG0_GPIO40 |
|-------------|-------------|

| | |
|-----------------------|-----------|
| JP406 (2-3) (Default) | User LED1 |
|-----------------------|-----------|

Selecting JP406 position 2-3 allows use of the on board user led LED1 (D401)

4. Zero Ohm Links

CAN Load Resistor

| | |
|-------|---|
| JP501 | This link when inserted includes a 120 ohm resistor across CANH0 and CANL0. The default is connected. |
|-------|---|

AN_REF

| | |
|------|--|
| R101 | This zero ohm link when inserted provides a 3.3V reference for the EDP platform. The 3.3V used is the local supply voltage derived from a local voltage regulator. This link should be used in the absence of a 3.3V voltage reference voltage provided by the Analogue Module when fitted. The default position is not connected. |
|------|--|

AGND & VAGND

| | |
|------|--|
| R102 | This link when inserted provides a way of connecting the VAGND to the SGND. This is the default position. The two grounds alternatively can be connected to each other on the analogue module. |
|------|--|

5. Software Support

The NXP Command Module for the RS-EDP platform is supported by all of the necessary software drivers to make driving of the platform very easy. All the low level support for the devices controlled by I2C for example have been written, as well as a test menu to exercise each of the modules independently of the others. This therefore provides working example of the code which will allow students and users to cut and paste various sections into their own applications.

Each Applications Module has its own header file which provides the support for the functions that control it. Each module has its own set of high level functions that can be called to operate and control the hardware. This makes life a lot easier for the user, who can then spend most of his time working at the higher level application layer.

The software has been packed up as several ZIP file which can be downloaded and unpacked. Most of the projects have been written for the Keil uVision environment.

The majority of the applications written use the serial comm. channel ASC0 for outputting data to a terminal emulator. With this in mind a serial terminal emulation program should be used to read traffic outputted from the RS-EDP platform. Hyper Terminal is included in windows as part of the Windows Operating system but this does not work reliability. With this in mind it may be worth looking at other terminal emulator especially if they are to be used with USB-RS232 converters.

The terminal emulator should be set up for

115,200 baud
8 data bits
no stop bit
no parity
No flow control

The default jumper options for JP439 and JP430 should be left in place to ensure serial traffic is routed to the communication module. Always check the software to see if the baud rate has been changed.

Some of the provided software includes...

5.1 RSEDP_Test_Suite

This software exercises the NXP LPC1768 MCU peripherals including the on board ADC, PWM output, input capture, I2C, CAN, and I/O. The software also allows you to exercise the basic Application Modules, which are the Communication Module, the Digital I/O Module, and the Analogue Module. A suite of drivers and test menus are provided to fully exercise all the hardware on these boards.

5.2 MC1_Test_Suite

This is similar to the RSEDP_Test_Suite, but the test menus provided are for the MC1 Brushed DC Motor Drive Application Module. The motors are nominally 12V brushed DC motors running in a full H bridge configuration. The test suite allows you to accelerate the motor, change its direction, turn the brake on and off, as well as allowing the monitoring of motor current, DC link voltage and tacho feedback signals. The MC1 motor drive module also has many external inputs for limit switch detection and conditioning of motor related stimuli. The provided software library will therefore allow you to fully exercise your motor.

5.3 MC2_Test_Suite

This is similar to the MC1 test suite but for brushless DC/AC motors. The software assumes you have an MC2 motor drive module fitted, and you want to communicate to it via I2C packets. This set of software therefore allows you communicate with the MC2 motor drive module across the I2C backplane network, present in the RSEDP system. You can have up to three MC2 motor drives fitted and this suite of software allows you to communicate with all of them.

5.4 Easy Web

This piece of software allows the NXP processor to serve a web page via its on board Ethernet port. The software allows you to effectively test the Ethernet port is working correctly. The software was written by Andreas Dannenberg at the University of Applied Science in Germany, and has been modified to work on the RSEDP platform.

By using these suites of software you can fully exercise the RS-EDP platform to ensure all of the items are working correctly. You can also use the software as building blocks for your own projects.